

Integrated Multi-Channel DC-DC Converters for Panels

Description

The FP9929A offers a compact power supply solution to provide all voltages required by EPD panel. The FP9929A includes 2 high performance PFM DC-DC converters, one is for positive voltage and the other is for negative voltage used by EPD drivers, a VCOM buffer (unity-gain OPA), a positive charge pump and a negative charge pump to provide adjustable regulated output voltages.

The converters provide the regulated positive and negative supply voltage for the panel source driver ICs.

The positive charge pump controller provides regulated EPD gate-on voltage. The negative charge pump controller provides regulated EPD gate-off voltage.

Accurate back-plane biasing is provided by a linear amplifier and can be adjusted either by an external resistor or the I²C interface. The VCOM driver can source or sink current depending on panel condition. For automatic VCOM adjustment in production line, VCOM can be set from -0.6V to -5V with 8 bit control through the serial interface.

The FP9929A provides precise temperature measurement function to monitor the panel temperature during operation.

Pin Assignments

Package (TQFN-32)(5mm×5mm)

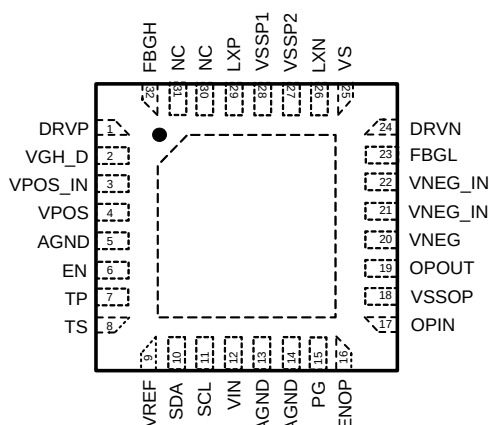


Figure 1. Pin Assignment of FP9929A

Features

- High Efficiency
- Low Power Consumption
- 2.7V to 5.5V Input Supply Voltage
- I²C Serial Interface
- Over-Temperature Protection

DC-DC Converters

- Fast Transient Response to Pulsed Load
- Built-In 20V, 5A, 0.25Ω MOSFET
- Built-In Soft-Start
- Over-Current Protection

LDO Regulator

- Built-In ±15V LDO with ±0.15V accuracy for Source Driver Supply

Adjustable VCOM Driver for Accurate Panel-Backplane Biasing

- -0.6V to -5V
- 8-bit Control

Regulated Charge Pumps

- Charge Pump for VGH Regulation
- Charge Pump for VGL Regulation
- TQFN-32 (5mm×5mm) Package
- RoHS Compliant

Thermistor Monitoring

- -10°C to +85°C Temperature Range
- ±3°C Accuracy from 0°C to 50°C (IC=25°C)

Applications

- Electro-Phoretic Display (EPD) Panel
- E-Book
- P-DVD
- CAR TV

Ordering Information

FP9929A□

Package Type
WB: TQFN-32 (5mm×5mm)

Typical Application Circuit

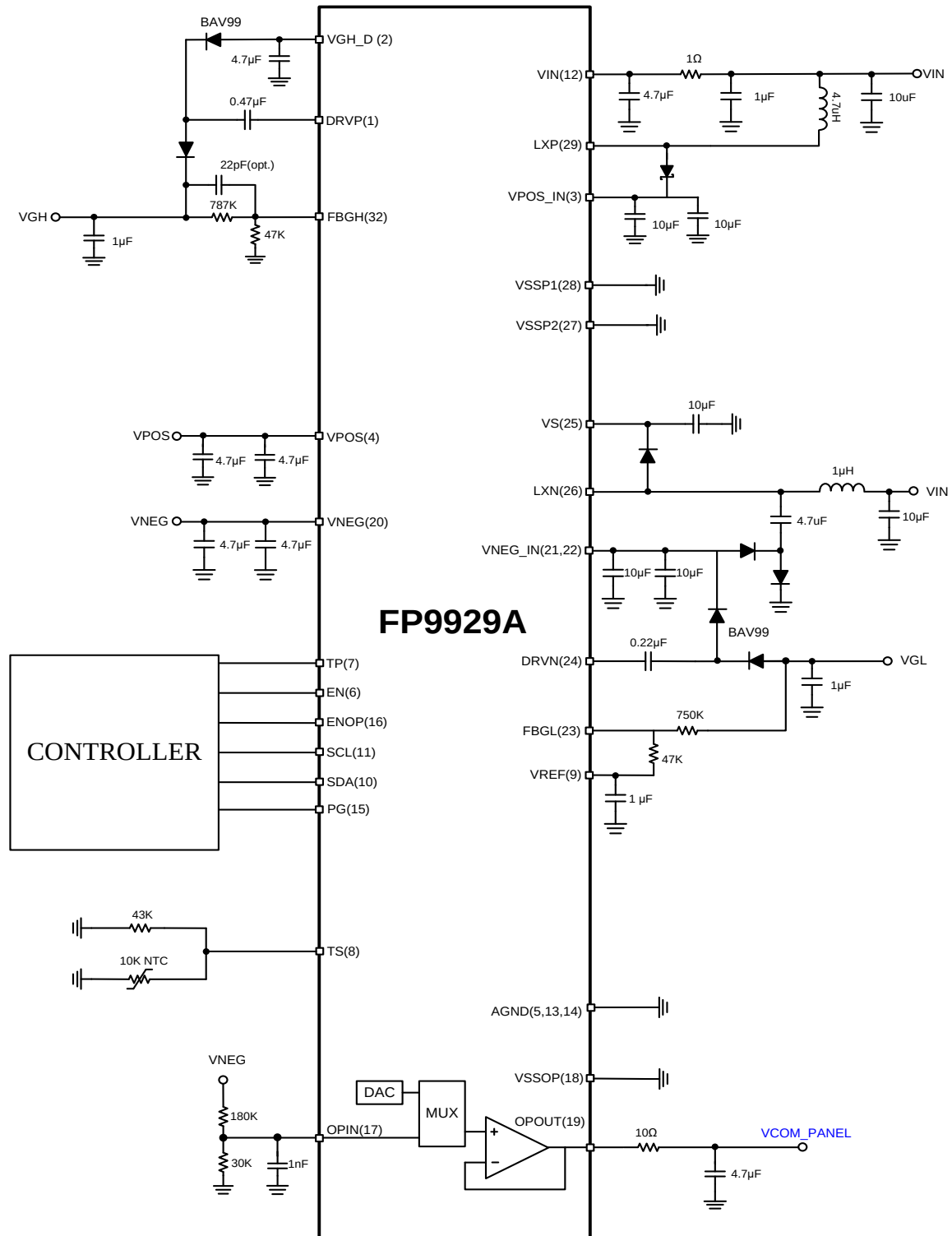


Figure 2. Typical Application Circuit of FP9929A

Functional Pin Description

Pin Name	Pin No.	Pin Function
DRVP	1	Switching Pin. Driver for the positive charge pump.
VGH_D	2	Base voltage output pin for positive charge pump.
VPOS_IN	3	Input pin for VPOS(LDO)
VPOS	4	Positive supply output pin.
AGND	5	Analog GND
EN	6	Enable Pin of Whole CHIP
TP	7	Test pin for testing, please do not connect to any signal.
TS	8	Thermistor input pin. Connect a 10K NTC thermistor and a 43K linearization resistor between this pin and system GND.
VREF	9	Internal Reference Bypass Terminal.
SDA	10	Serial interface (I2C) data input/output.
SCL	11	Serial interface (I2C) clock input.
VIN	12	Power Supply Input. The supply voltage powers all the control circuits.
AGND	13	Analog GND
AGND	14	Analog GND
PG	15	Power Good singal
ENOP	16	Enable Pin of Unity-Gain Operational Amplifier, active when EN is high.
OPIN	17	Unity-Gain Operational Amplifier Input Pin.
VSSOP	18	Positive Supply of Unity-Gain Operational Amplifier.
OPOUT	19	Unity-Gain Operational Amplifier Output Pin.
VNEG	20	Negative Source Driver Power, also ground of op-amp.
VNEG_IN	21	Input pin for LDO (VNEG).
VNEG_IN	22	Input pin for LDO (VNEG).
FBGL	23	Voltage Feedback to Determine Negative Charge Pump Output Voltage. FBGL is regulated to 0V.
DRVN	24	Switching Pin. Driver for the negative charge pump.
VS	25	Regulated voltage for internal circuit
LXN	26	Switching Pin.Drain of the internal power NMOS for the negative regulator.
VSSP2	27	Power Ground. VSSP2 is the source of negative boost converter power NMOS.

VSSP1	28	Switching Pin. Drain of the internal power NMOS for the positive regulator.
LXP	29	Power Ground. VSSP1 is the source of positive or Inverting boost converter power NMOS.
NC	30	Reserved.
NC	31	Reserved.
FBGH	32	Base voltage output pin for positive charge pump.

Block Diagram

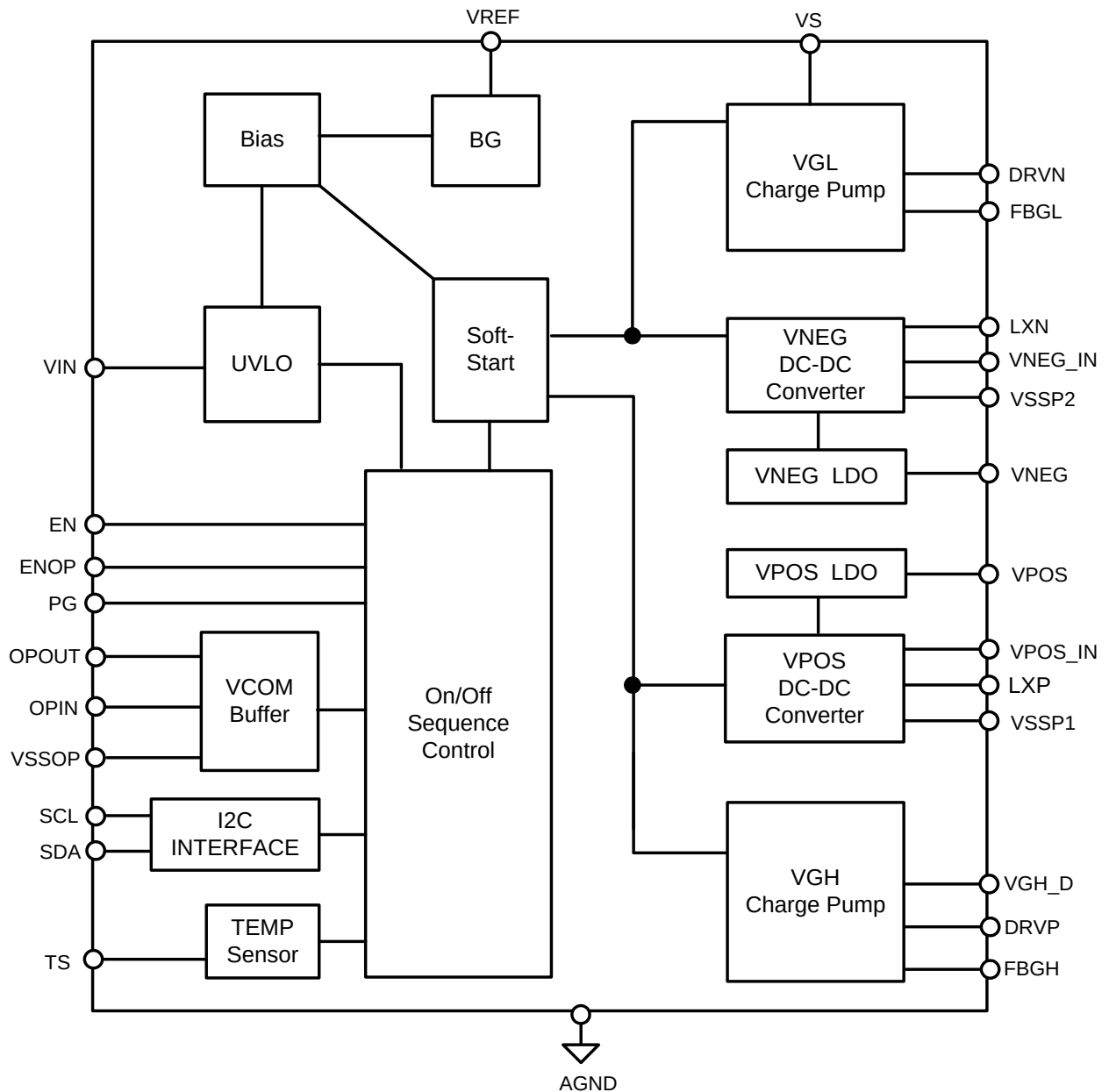


Figure 3. Block Diagram of FP9929A

Absolute Maximum Ratings

- DRVP, DRVN, LXP, LXN, VPOS_IN, VPOS, VGH_D, VS ----- -0.3V to +22V
- FBGH, TP, TS, VIN, VREF, FBGL, ----- -0.3V to +6V
- SCL, SDA, EN, ENOP, PG ----- -0.3V to +6V
- VNEG_IN, VNEG, OPIN, OPOUT ----- -24V to +0.3V
- VSSP1, VSSOP2, VSSOP ----- -0.3V to +0.3V
- Power Dissipation @ $T_A=25^{\circ}\text{C}$, (P_D)
 - TQFN-32 (5mm×5mm) ----- 2.3W
- Package Thermal Resistance, (θ_{JA})
 - TQFN-32 (5mm×5mm) ----- 36°C/W
- Lead Temperature (Soldering, 10sec.) ----- $+260^{\circ}\text{C}$
- Maximum Junction Temperature (T_J) ----- $+150^{\circ}\text{C}$
- Storage Temperature (T_{STG}) ----- -65°C to $+150^{\circ}\text{C}$

Note : Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage (VIN) ----- +2.7V to +5.5V
- Operating Junction Temperature Range ----- -40°C to $+85^{\circ}\text{C}$

Electrical Characteristics

($V_{IN}=3.7V$, typical values are at $T_A=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
System Supply						
Input Voltage Range	V _{IN}		2.7	3.7	5.5	V
V _{IN} UVLO Threshold	V _{UVLO}	V _{IN} Rising	-	2.5	-	V
		Hysteresis	-	0.2	-	
V _{IN} Supply Current	I _{IN}		-	1.5	-	mA
V _{IN} Shutdown Current	I _{SD}		-	0.1	1	μA
REF Output Voltage	V _{REF}		1.225	1.25	1.275	V
Thermal Shutdown Threshold	T _{SD}		-	140	-	°C
		Hysteresis	-	20	-	°C
Boost Regulator						
NMOS Switch ON-Resistance	R _{ONNMOS}		-	0.25	-	Ω
NMOS Switch Current Limit	I _{LIMNMOS}		-	5	-	A
NMOS Switch Leakage Current	I _{LXNMOS}	V _{LXP} =18V	-	0.1	-	μA
VPOS LDO						
Input Voltage Range	V _{POS_IN}			17		V
Output Voltage Range	V _{POS}		14.7	15	15.3	V
Current Limit	I _{LIMIT}		200	--	--	mA
Inverting Regulator						
NMOS Switch ON-Resistance	R _{ONNMOS}		-	0.25	-	Ω
NMOS Switch Current Limit	I _{LIMNMOS}		-	5	-	A
Switch Leakage Current	I _{LXNMOS}	V _{LXN} =18V	-	0.1	-	μA
VNEG LDO						
Input Voltage Range	V _{NEG_IN}			-17		V
Output Voltage Range	V _{NEG}		-15.3	-15	-14.7	V
Current Limit	I _{LIMIT}		200	--	--	mA

Electrical Characteristics

($V_{IN}=3.7V$, typical values are at $T_A=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCOM Buffer						
Accuracy	V_{COMACC}	$VCOM_SET[7:0]=0x74h(-2.5V)$ $V_{IN}=3.7V$, No load	-1.5		1.5	%
Output voltage range	V_{COM}		-5		-0.6	V
Resolution	V_{RES}	$VCOM_ADJ=1$, 1 LSB	-	22	--	mV
VCOM Gain (OPOUT/OPIN)	V_G	$VCOM_ADJ=0$	-	1	--	V/V
POSITIVE CHARGE PUMP						
Input Voltage Range				17		V
Postive Feedback Voltage	V_{FBGH}		--	1.25	--	V
VFB Accuracy	V_{FBGHA}		-2		2	%
Output voltage range	V_{GH}		20		30.5	V
DP ON-R High	$R_{DS(ON)}$		--	5	--	Ω
DP ON-R LOW	$R_{DS(ON)}$		--	3	--	Ω
NEGATIVE CHARGE PUMP						
Input Voltage Range				-17		V
Negative Feedback Voltage	V_{FBGL}		--	0	--	V
VFB Accuracy	V_{FBGLA}		-40		40	mV
Output voltage range	V_{GL}		-25		-20	V
DN ON-R High	$R_{DS(ON)}$		--	5	--	Ω
DN ON-R LOW	$R_{DS(ON)}$		--	3	--	Ω

Electrical Characteristics

($V_{IN}=3.7V$, typical values are at $T_A=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LOGIC LEVELS AND TIMING CHARACTERISTIC (SCL, SDA)						
Input Low Threshold Level	V_{IL}		-	-	0.4	V
Input High Threshold Level	V_{IH}		1.2	-	-	V
Output Low Threshold Level	V_{OL}	$I_O=3mA$, Sink Current.	-	-	0.4	V
SCL Clock Frequency	f_{SCL}		-	-	400	kHz
Thermal Sensor (Note 1)						
Offset	OffsetTMS	Temperature = $25^{\circ}C$	-	1.18	-	V
Maximum Input Level	VTMS_MAX		-	2.25	-	V
Internal Pull Up Resistor	RNTC_UP		-	7.307	-	K Ω
External Linearization Resistor	RLINEAR		-	43	-	K Ω

Note 1: 10K Ω Murata NCP18XH103F03RB thermistor (1%) in parallel with a linearization resistor (43k Ω , 1%) are used at TS pin for panel temperature measurement.

Power On Sequence

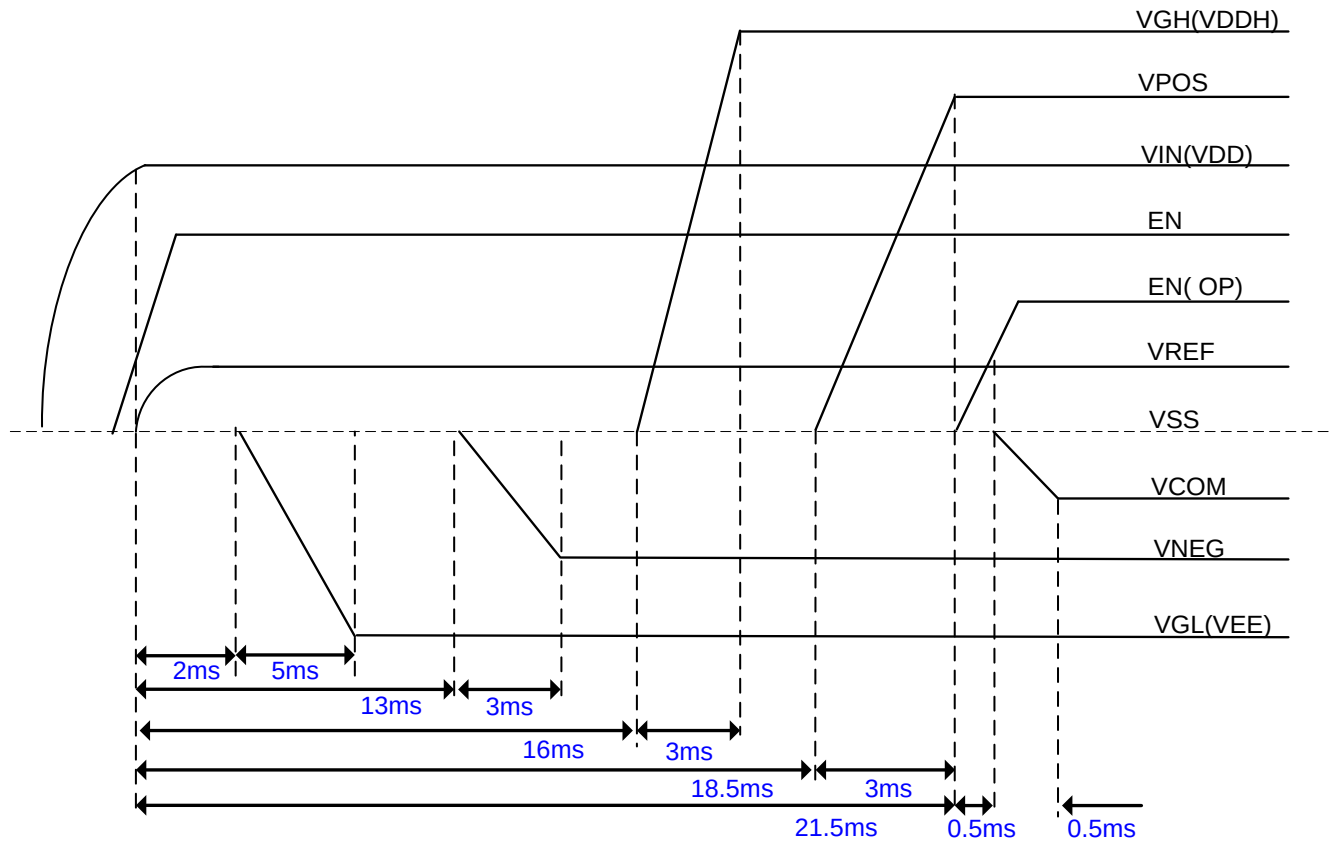


Figure 4. Power-on Sequence

The diagram shows the timing relationships for the VDDH pin. The signals and their levels are:

- VGH (VDDH)**: High voltage level.
- VPOS**: Positive voltage level.
- VIN (VDD)**: Input voltage level.
- EN (Power)**: Enable signal for power.
- EN (VCOM)**: Enable signal for VCOM.
- VSS**: Ground reference level.
- DATA**: Data signal.
- VCOM**: Common mode voltage.
- VNEG**: Negative voltage level.
- VGL (VEE)**: Low voltage level.

Key timing parameters and voltage levels are indicated:

- VHD**: High voltage duration.
- VPD**: Voltage level for VPD.
- VCD**: Voltage level for VCD.
- VND**: Voltage level for VND.
- 7.4V**: Specific voltage level for VCD.
- TDV**: Time delay from VGL to VCD.
- VLD**: Voltage level duration.

Variables	Min	max	Remark
TDV	100us	-	
VHD	0s	-	
VPD	0s	-	
VND	0s	-	
VCD	0s	-	
VLD	500ms	-	Discharge point at -7.4V

I2C Address

The IC is a slave-only device and responds to the 7-bit address 90h. A0 :1 indicating read(91h), and 0 indicating write(90h)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	R/W

Register Address Map

Register	Address (Hex)	Name	Default Value	Description
0	0x00	TMST_VALUE	N/A	Thermistor value read by ADC
1	0x01	FUNC_ADJUST	0000 0001	Vcom output adjustment method and I ² C read pointer control
2	0x02	VCOM_SETTING	0111 0100	Voltage setting for Vcom

THERMISTOR READOUT (TMST_VALUE)

Address – 0x00h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	TMST_VALUE [7:0]							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	NA	NA	NA	NA	NA	NA	NA	NA

Field Name	Bit Definition
TMST_VALUE [7:0]	Temperature read-out 1111 0110 – < -10°C 1111 0110 – -10°C 1111 0111 – -9°C --- 1111 1110 – -2°C 1111 1111 – -1°C 0000 0000 – 0°C 0000 0001 – 1°C 0000 0010 – 2°C --- 0001 1001 – 25°C --- 0101 0101 – 85°C 0101 0101 – > 85°C

VCOM ADJUSTMENT METHOD and I²C read pointer control (FUNC_ADJUST)

Address – 0x01h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Not Used							VCOM_ADJ[0]
Read/Write	R	R	R	R	R	R	R	R./W
Reset Value	NA	NA	NA	NA	NA	NA	NA	1

Field Name	Bit Definition
VCOM_ADJ	VCOM output adjustment method 0 – OPIN pin 1 – I²C interface (Default)

VCOM ADJUSTMENT (VCOM_SETTING)

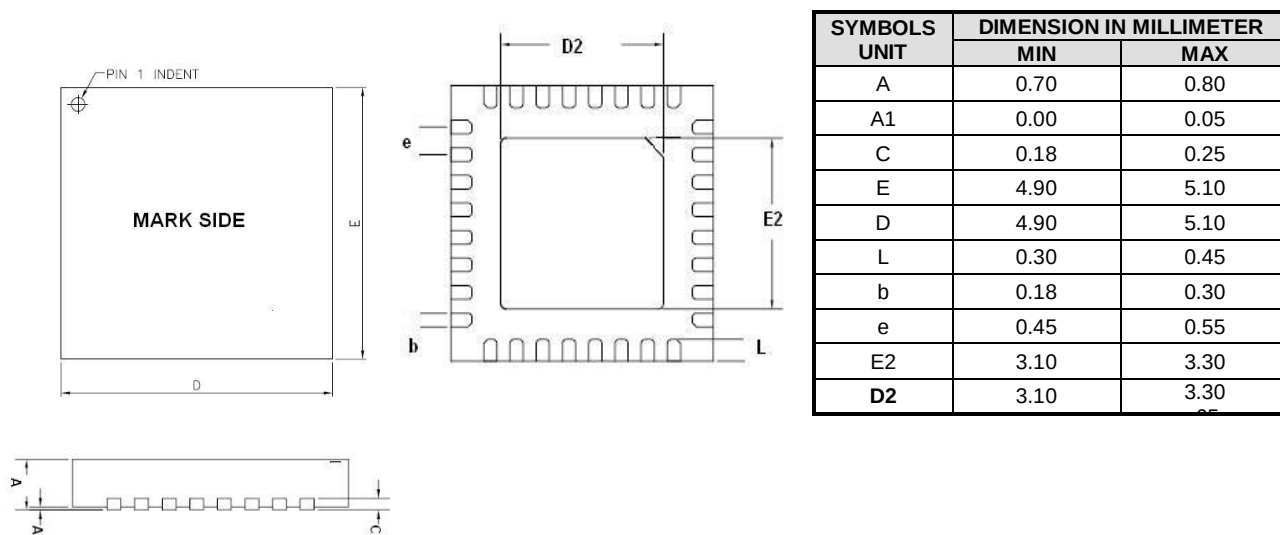
Address – 0x02h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VCOM_SET[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	1	1	0	1	0	0

VCOM DAC	Setting Voltage	VCOM DAC	Setting Voltage	VCOM DAC	Setting Voltage
00H	Reserved				
01H	Reserved				
02H	Reserved				
03H	Reserved			E8H	-5002mV
04H	Reserved				Reserved
05H	Reserved				Reserved
06H	Reserved				Reserved
07H	Reserved	73H	-2478mV		Reserved
08H	Reserved	74H	-2500mV		Reserved
18H	Reserved	75H	-2522mV		Reserved
19H	Reserved				
1CH	-604mV				
1DH	-626mV				Reserved
1EH	-648mV			FE	Reserved

Outline Information

TQFN- 32 5mm×5mm (pitch 0.5mm)Package (Unit: mm)



Carrier dimensions

